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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,298	03/01/2004	Khoi A. Phan	H0266 / AMDP812US	9262
23623	7590	05/06/2009	EXAMINER	
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			ART UNIT	PAPER NUMBER
			2814	
			NOTIFICATION DATE	DELIVERY MODE
			05/06/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/790,298	Applicant(s) PHAN ET AL.	
	Examiner Abul Kalam	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 February 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5,7,23,25,26,33 and 34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5,7,23,25,26,33 and 34 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claim 34 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In lines 7-8 of claim 34, the limitation of "wherein each of thermo-electrical structures has a structure of line patterns selected from a group comprising: helix structure, and a spring structure," is unclear because limitation of thermo-electrical structures lacks antecedent basis.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-5, 7, 23, 25-27, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dhindsa et al. (US 5,740,016) in view of Saika (6,573,596) and Morris et al. (US 6,230,497).

Regarding claim 1, Dhindsa discloses in fig. 1, a heat regulating device for regulating a heat flow into and out of an integrated circuit semiconductor body comprising: a plurality of thermo-electrical (TE) structures (140), that creates a uniform temperature gradient (col. 4 lines 13-22) across an integrated circuit semiconductor body (120) via heat inducement to and/or dissipation of generated heat away from a portion of the integrated circuit semiconductor body wherein the thermo-electrical structures 140 is a composite, col. 3 lines 51-60, composed of a layer having at least one part tailored to a heat-generating characteristic of a portion of the integrated circuit semiconductor body (120) (col. 3, lines 51-60: "The thermoelectric device may comprise two elements formed of different electroconductive material connected by a junction, operating according to the Peltier effect").

at least one layer of a conductive material (160) in contact with the thermo-electrical structure (140) for conducting heat flow; and

at least one of plurality of the TE has a distribution line patterns wherein each of the thermo-electric structures (140) has a structure of patterns selected from a group comprising: helix structure and a spring structure (fig. 2a).

But, Dhindsa does not explicitly disclose:

a) wherein the thermoelectric structure has a distribution pattern that is a denser towards center of the structure and a less dense towards outer edges of the structure; and

b) wherein the at least one thermoelectric structure is coupled to an associated hot spot.

Regarding the limitation of the distribution pattern density, Dhindsa states that the TE structures 140, figs. 2a-2b, may be arranged in any desired pattern, col. 5, lines 45-50. Furthermore, Saika discloses a heat regulating device, fig. 2, with thermoelectric structures 12, figs. 5, wherein the distribution pattern of the structures is dense towards the center and less dense towards the outer edges of the structure, col. 6, lns. 15-26. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to incorporate the teaching of Saika into the device of Dhindsa, to form the thermoelectric structures in such a density gradient as claimed, for the purpose of improving thermal efficiency.

Regarding, the limitation of the hot spot, Morris teaches a heat regulating device, fig. 3, wherein the thermoelectric structures 38, are coupled to associated hot spots, figs. 4A-4C, col. 5, lns. 53-67, for the purpose of establishing an even temperature level throughout the device, col. 6, lns. 1-7. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to incorporate the teaching of Morris into the device of Dhindsa, to have the thermoelectric structures coupled to the associated hot spots, for the purpose of providing an even and near-uniform distribution of heat across the entire device.

Regarding claim 2, Dhindsa discloses the heat regulating device wherein the thermo-electrical structure (140) is trough within the body of the layer of the conductive material 160, fig. 1.

Regarding claims 3-5, Dhindsa discloses the heat regulating device further comprising a plurality of the thermo-electrical structures (140) connected form a

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spreading assembly, fig. 1, wherein the spreading assembly is operatively connected to a heat sink (170), fig. 1, wherein the thermo-electrical structure 140 is a conductive pathway for heat transfer.

Regarding claims 23 and 25-26, Dhindsa discloses the heat regulating device with components (140), embedded into the spreading assembly to manage the heat flow away from and/or into the portion of the semiconductor body of the integrated circuit, fig. 1, wherein the thermo-electrical structure (140) being embedded with measuring device (sensor) to measure various physical properties of the portion of the semiconductor body of the integrated circuit, col. 4, lns. 33-47, fig. 1, wherein the thermo-electrical structure 140 being external element attached to the surface of the heat regulating device, fig. 1.

Regarding claim 33, Dhindsa discloses a heat regulating device at least one thermo-electric structure 140, fig. 1, is integrated with the semiconductor body (120) such that the thermo-electrical structure (140) is positioned in a region of the semiconductor body where a hot spot (IC would generate heat) is anticipated.

Regarding claims 7 and 34, Dhindsa discloses a heat regulating device for regulating a heat flow of an integrated circuit comprising:

means (140, fig. 1) for inducing heat into a portion of a semiconductor body of the integrated circuit (120) utilizing a plurality thermo-electric structures (140, fig. 1), or a means (140) for dissipating heat away from the portion of the semiconductor region of a semiconductor body of the integrated circuit (120) utilizing a plurality of thermo-electric

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structures (140) wherein the thermo-electrical structures 140 is a composite, col. 3 lines 55-60, composed of a layer having at least one part tailored to a heat-generating characteristic of a portion of the integrated circuit semiconductor body (120) (col. 3, lines 55-60: "The thermoelectric device may comprise two elements formed of different electroconductive material connected by a junction, operating according to the Peltier effect");

the heat inducing means and/or heat dissipating means creates a uniform temperature gradient across the semiconductor body (col. 4 lines 13-22); means (160) for conducting heat in contact with the means (140) for inducing heat into or dissipating heat away from the portion of the semiconductor body of the integrated circuit (fig. 1); and least one of plurality of the TE has a distribution line patterns, wherein each of the thermo-electric structures (140) has a structure of patterns selected from a group comprising: helix structure and a spring structure (fig. 2a).

But, Dhindsa does not explicitly disclose:

a) wherein the thermoelectric structure has a distribution pattern that is a denser towards center of the structure and a less dense towards outer edges the structure; and

b) wherein the at least one thermoelectric structure is coupled to an associated hot spot; and

Regarding the limitation of the distribution pattern density, Dhindsa states that the TE structures 140, figs. 2a-2b, may be arranged in any desired pattern, col. 5, lines 45-50. Furthermore, Saika discloses a heat regulating device, fig. 2, with thermoelectric structures 12, figs. 5, wherein the distribution pattern of the structures is dense towards

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the center and less dense towards the outer edges of the structure, col. 6, Ins. 15-26. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to incorporate the teaching of Saika into the device of Dhindsa, to form the thermoelectric structures in such a density gradient as claimed, for the purpose of improving thermal efficiency.

Regarding, the limitation of the hot spot, Morris teaches a heat regulating device, fig. 3, wherein the thermoelectric structures 38, are coupled to associated hot spots, figs. 4A-4C, col. 5, Ins. 53-67, for the purpose of establishing an even temperature level throughout the device, col. 6, Ins. 1-7. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to incorporate the teaching of Morris into the device of Dhindsa, to have the thermoelectric structures coupled to the associated hot spots, for the purpose of providing an even and near-uniform distribution of heat across the entire device.

Response to Arguments

3. Applicant's arguments filed February 17, 2009, have been fully considered but they are not persuasive.

With respect to the Dhindsa reference, Applicant argues:

"the cited passage makes no reference to wherein each of the thermo-electrical structures is a composite composed of a layer having at least one part tailored to a heat generating characteristic of a portion of the integrated circuit semiconductor body."

The argument is not persuasive. In column 5, lines 51-65, Dhindsa discloses:

"The thermoelectric device may comprise two elements formed of different electroconductive material connected by a junction, operating according to the Peltier effect...by having an appropriate design of the substrate support using multiple

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thermoelectric modules at different locations on the substrate support, the temperature gradient across the substrate support surface can be controlled." Thus, Dhindsa does disclose wherein the thermo-electric structures is a composite with at least on part tailed to a heat generating characteristic of the semiconductor body.

Applicant also argues that each portion of the layer disclosed in the claimed subject matter is formed of a various material that provides "**different heat-generating characteristic.**" Note that such a feature is not recited in the claim. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is (571)272-8346.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K./
Examiner, Art Unit 2814

/Phat X. Cao/
Primary Examiner, Art Unit 2814